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Terms	Documents
L4 and (low near2 K)	5

Database:

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- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search:

L5

[Refine Search](#)[Recall Text](#)[Clear](#)**Search History**DATE: Monday, April 21, 2003   [Printable Copy](#)   [Create Case](#)Set Name   Query  
side by sideHit Count   Set Name  
result set*DB=USPT; PLUR=YES; OP=ADJ*

<u>L5</u>	L4 and (low near2 K)	5	<u>L5</u>
<u>L4</u>	L3 and (low adj dielectric)	33	<u>L4</u>
<u>L3</u>	L2 and (gate near2 contact)	1066	<u>L3</u>
<u>L2</u>	L1 and ( second near2 contact)	4259	<u>L2</u>
<u>L1</u>	fet or (field adj effect adj transistor)	66854	<u>L1</u>

END OF SEARCH HISTORY

**WEST**[Generate Collection](#)[Print](#)**Search Results - Record(s) 1 through 5 of 5 returned.**☐ 1. Document ID: US 6534837 B1

L5: Entry 1 of 5

File: USPT

Mar 18, 2003

US-PAT-NO: 6534837

DOCUMENT-IDENTIFIER: US 6534837 B1

TITLE: Semiconductor device

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
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☐ 2. Document ID: US 6492249 B2

L5: Entry 2 of 5

File: USPT

Dec 10, 2002

US-PAT-NO: 6492249

DOCUMENT-IDENTIFIER: US 6492249 B2

TITLE: High-K gate dielectric process with process with self aligned damascene contact to damascene gate and a low-k inter level dielectric

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 3. Document ID: US 6291278 B1

L5: Entry 3 of 5

File: USPT

Sep 18, 2001

US-PAT-NO: 6291278

DOCUMENT-IDENTIFIER: US 6291278 B1

TITLE: Method of forming transistors with self aligned damascene gate contact

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 4. Document ID: US 6271132 B1

L5: Entry 4 of 5

File: USPT

Aug 7, 2001

US-PAT-NO: 6271132

DOCUMENT-IDENTIFIER: US 6271132 B1

TITLE: Self-aligned source and drain extensions fabricated in a  
damascene contact and gate process

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC
Draw Desc	Image										

☐ 5. Document ID: US 5935766 A

L5: Entry 5 of 5

File: USPT

Aug 10, 1999

US-PAT-NO: 5935766

DOCUMENT-IDENTIFIER: US 5935766 A

TITLE: Method of forming a conductive plug in an interlevel  
dielectric

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	KWIC
Draw Desc	Image									

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Terms	Documents
L4 and (low near2 K)	5

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